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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,073	09/18/2003	Takashi Naiki	81876.0058	6849

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HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 04/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,073	NAIKI, TAKASHI	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, another IC chip as claimed in claim 22 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 22 is objected to because of the following informalities: the terminology of substrate/another IC chip is informal and should be replaced with "or". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,278,128 Noji et al. in view of Japanese Patent No. 63-122150 Yamaguchi.

3. Referring to claim 19, an IC chip comprising at least one externally and selectively cuttable member, (Noji et al. Figure 6a #96), having at least one cuttable section, (Noji et al. Figure 6a narrow part of #96), the cuttable member, (Noji et al. Figure 6a #96), including a multiplicity of cuttable points, (Yamaguchi Figure 1 #3 and see **), wherein said cuttable member remain cut open so long as at least one cuttable point remains cut open, and wherein said cuttable member includes a multiplicity of cuttable sections which are coupled at one ends thereof with the same electric potential and coupled at the other ends thereof with respective logic circuits, (Noji et al. Figure 9).

** Noji et al. teaches all of the claimed matter except for the teachings of multiple cuttable sections in the cuttable member, but Yamaguchi does. Yamaguchi et al. teaches all of the claimed matter except for the teachings of the member being connected to as logic circuit. It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings of Yamaguchi with the teachings of Noji et al. because by making the cuttable member have multiple cutting points allows the member to be cut in another area if the first area was unable to be cut because of a dust particle or the like deposited in the first area, (Yamaguchi Japanese Patent Abstract Constitution Lines 5-10).

4. Referring to claim 20, an IC chip, wherein said cuttable sections have a linear portion of a uniform width, (Noji et al. Figure 6A #96 the narrow section of the fuse and Yamaguchi Figure 1 #3).

5. Referring to claim 21, an IC chip, wherein each of said cuttable sections has a narrow portion, (Noji et al. Figure 6A #96 the narrow section of the fuse and Yamaguchi Figure 1 #3),

formed between two wide portions, (Noji et al. Figure 6A #96 the wide section of the fuse and Yamaguchi Figure 1 area of #2).

6. Referring to claim 22, a semiconductor device, comprising: an IC chip having at least one externally and selectively cut member, (Noji et al. Figure 6a #96), including at least one cut section, (Noji et al. Figure 6a narrow part of #96), the cut member, (Noji et al. Figure 6a #96), including a multiplicity of cut points, (Yamaguchi Figure 1 #3 and see **), said cut member working normally when at least one of said cut points remains cut open, (Yamaguchi Figure 1 #3 and see **), and bumps, (Noji et al. Figure 6a&b #78), formed on the same side of the IC chip, (Noji et al. Figure 6a&b #62), as the cut member in association with respective cut points, (Noji et al. Figure 6A #96 the narrow section of the fuse and Yamaguchi Figure 1 #3); a substrate/another IC chip, (Noji et al. Figure 12); and a connection member made of an anisotropic conductor, (Yamaguchi Japanese Patent Abstract Constitution Lines 1-5 and SEE ***), and sandwiched between said IC chip and said substrate/another IC chip, (Noji et al. Figure 12), wherein said IC chip and said substrate/another IC chip, (Noji et al. Figure 12) are pressed together, and wherein said cut member, (Noji et al. Figure 6a #96), includes a multipliclty of cut sections, (Yamaguchi Figure 1 #3 and see **), which are coupled at one ends thereof with the same electric potential and coupled at the other ends thereof with respective logic circuits, (Noji et al. Figure 9).

** Noji et al. teaches all of the claimed matter except for the teachings of multiple cuttable sections in the cuttable member, but Yamaguchi does. Yamaguchi et al. teaches all of the claimed matter except for the teachings of the member being connected to as logic circuit. It would have been obvious to one having skill in the art at the time the invention was made to

combine the teachings of Yamaguchi with the teachings of Noji et al. because by making the cuttable member have multiple cutting points allows the member to be cut in another area if the first area was unable to be cut because of a dust particle or the like deposited in the first area, (Yamaguchi Japanese Patent Abstract Constitution Lines 5-10).

*** Noji et al. discloses the claimed invention except for the material of the cuttable members and more specifically being made out of an anisotropic material, but Yamaguchi does. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the cuttable members out of an anisotropic material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

7. Referring to claim 23, a semiconductor device, wherein said cut sections have a linear portion of a uniform width, (Noji et al. Figure 6A #96 the narrow section of the fuse and Yamaguchi Figure 1 #3).

8. Referring to claim 24, a semiconductor device, wherein each of said cut sections has a narrow portion, (Noji et al. Figure 6A #96 the narrow section of the fuse and Yamaguchi Figure 1 #3), formed between two wide portions, (Noji et al. Figure 6A #96 the wide section of the fuse and Yamaguchi Figure 1 area of #2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

VAMJ
3/31/04